**AKGEC/IAP/FM/02**

**Ajay Kumar Garg Engineering College, Ghaziabad**

**Department of ECE**

**Sessional Test-2**

Course: B.Tech Semester: I

Session: 2017-18 Section: EI, EN, CS, IT

Subject: Basic Electronics Sub. Code: REC 101

Max Marks: 50 Time: 2 hour

***Note*** : Answer **all** the sections.

**Section-A**

1. Attempt **all** the parts. **(5x2 = 10)**
2. Explain why BJT is a bipolar device?
3. Explain FET as a Voltage Variable Register.
4. List the ideal characteristics of OP-AMP.
5. The BJT has IC = 10mA and α = 0.98. Determine the value of β and IB.
6. List the primary difference between JFET and MOSFET.

**Section-B**

1. Attempt **all** the parts. **(5x5 = 25)**
2. Draw the CE configuration circuit of BJT and explain its input and output characteristics.
3. Determine the dc bias voltage VCE and the current IC for the voltage-divider configuration of Fig.1

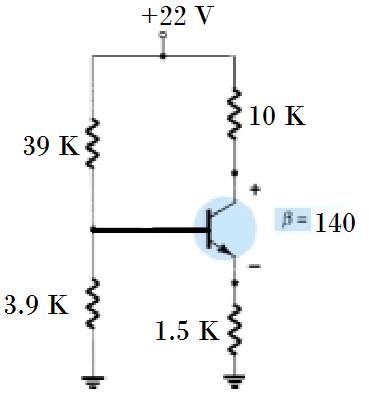


Fig.1

1. Derive the stability factor S(ICO) for the emitter bias configuration.
2. Define Slew Rate and determine the output voltage of a differential amplifier for the input voltages of 300µV and 240µV. The differential gain of the amplifier is 5000 and the value of CMRR is 100.
3. Draw the structure of n-channel JFET and explain its principle of operation with its V-I characteristics.

P.T.O.

**Section-C**

1. Attempt **all** the parts. **(2x7.5 = 15)**
   1. Distinguish between enhancement type and depletion type MOSFETs.
   2. Determine VGS , ID and VDS for the network of Fig.2 if IDSS = 8 mA, VP = -- 6 V,

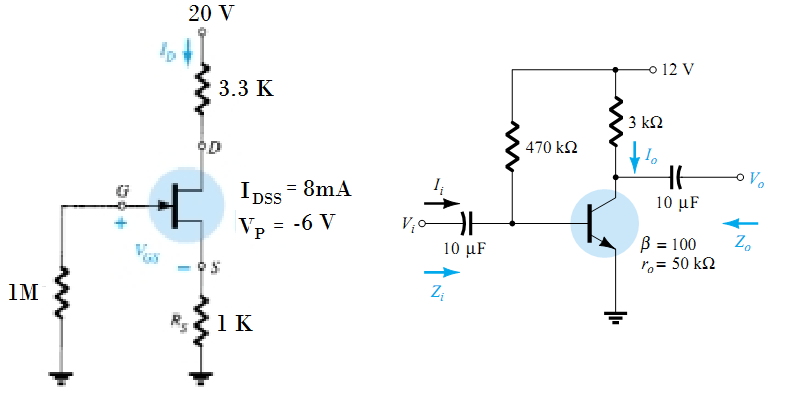


Fig.2 Fig.3

* 1. Determine re, Zi, Zo, Av and Ai for the given circuit shown in fig.3 with ro = 50 K.
  2. Determine the output voltage for the circuit of Fig.4

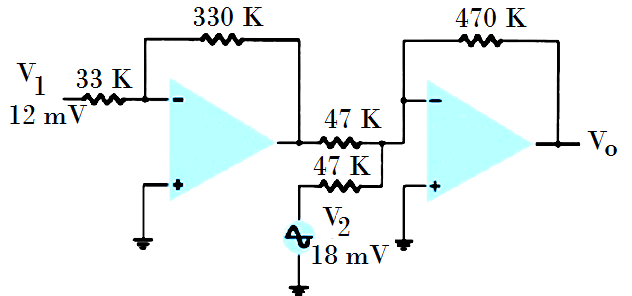


Fig. 4

* 1. Explain Integrator and Differentiator using OP-AMP.
  2. Draw block diagram of OP-AMP and equivalent circuit of OP-AMP and explain.